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This work, done in collaboration with the European Council for Nuclear Research (CERN) and the University of Malta, presents the development of a new electronic front-end readout system for the High Momentum Particle Identification detector (HMPID) and the Charged Particle Veto (CPV) detector. The upgrade strategy for the A Large Ion Collider Experiment (ALICE) is based on the collection of more than 10 nb^{-1} Pb-Pb collisions at a luminosity of 6 x 10^{27} cm^{-2} s^{-1}, corresponding to a collision rate of 50 kHz for Pb-Pb and 200 kHz for pp and p-Pb. The requirements for such a high luminosity cannot be met with the existing CPV electronics, which have a low readout rate of 5 kHz.

Considering the requirements and architectural complexity of such physics detectors in terms of hardware and firmware, the development of such a system is a challenging task and had to be completed within a time frame of two years. Therefore, different technologies and architectural topologies were considered and investigated for the optimization of the CPV front-end readout electronics. This work contributed to the development of a new custom front-end readout electronics system architecture for the CPV detector module in the PHOton spectrometer (PHOS). The redevelopment of this new front-end readout electronics architecture was commissioned and installed on the PHOS-CPV detector in November 2020.

Compared to the previous CPV and HMPID readout electronics, the proposed new architecture enables parallel readout and processing of all 480 silicon photomultiplier pads connected to digital signal processing boards. The new architecture includes the use of high-pin-count, low-power 28-nm FPGA technology for simultaneous readout of digital signal processors and the implementation of high-speed 3.125 Gbps transceiver links for data transfer from the front-end electronics to a remote readout module. In addition, the newly developed FPGA firmware architecture has helped increase the event readout rate and data throughput by a factor of ten. In addition, this work has contributed to the development of a new application-specific integrated circuit (ASIC) that includes four digital signal processors, error correction and detection circuits, and four serial transmitters with a bandwidth of at least 0.5 Gbps. The ASIC chip uses XFAB-180-nm technology and can process at least 192 analogue channels simultaneously. The developed ASIC device can be easily integrated into CPV, HMPID and similar electronic readout circuits for particle detectors. It also provides the ability to connect various front-end analogue-to-digital converters used in various data acquisition applications. In addition, this work has been published in five conference proceedings and one journal.

This research work is funded by the Tertiary Education Scholarships Scheme.